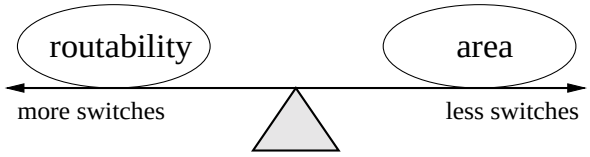
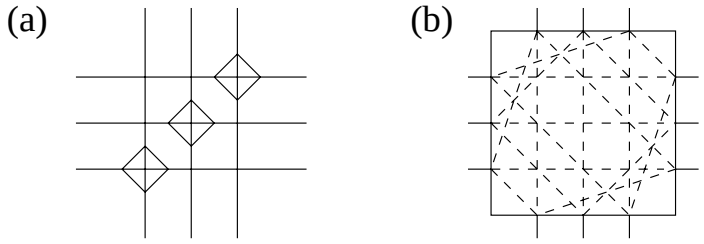
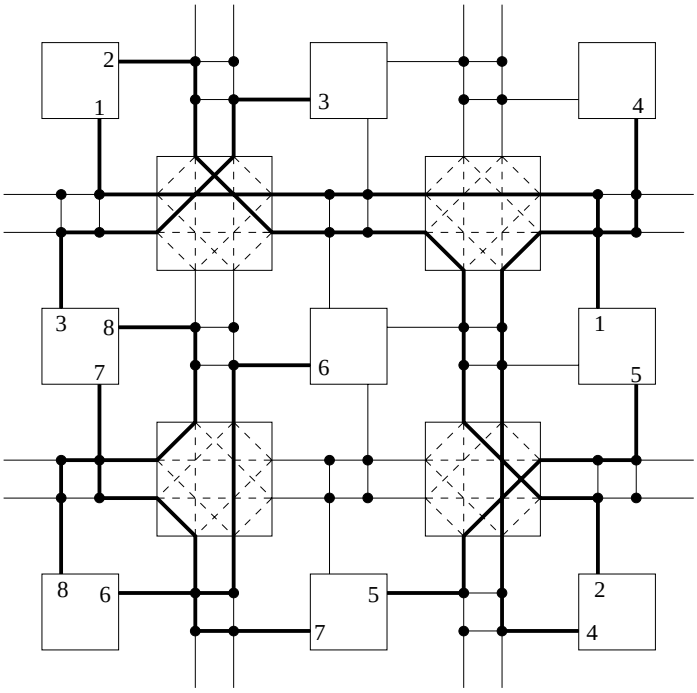
The Importance of Routing Resources in FPGA

- The routing resources of a FPGA are made up of prefabricated wire segments and programmable switches.
- Feasibility of FPGA design is constrained more by routing resources than by logic resources.
- Routing delays most limit the performance of FPGAs.
- Careful design of *switch modules* is of great importance.
- The intersection area of horizontal and vertical channels is referred to as switch module which is populated with programmable switches.
- Need to maximize routability under area (total # of switches) constraints.





(a) Xilinx XC4000-type switch module. (b) Its abstract representation showing what terminals can be connected.

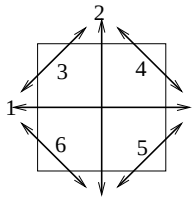


A routing instance. The structure of the switch module dictates which wire segments can be connected.

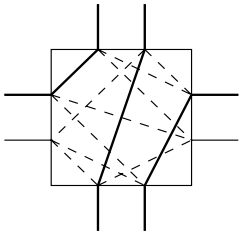
Switch Module Design

- Programmable switches usually occupy large areas, so the number of switches that can be placed in a switch module is limited.
- F_S (the flexibility of a switch module) is defined as the number of programming switches between one terminal and others. (Hence, there are $2 \times F_S \times W$ switches in a switch module.)
- A switch module M with W terminals on each side is said to be *universal* if every set of nets satisfying the dimensional constraints, i.e., number of nets on each side of M is at most W, is simultaneously routable through M.
- Switch module with $F_S = 3$ ($6W$ switches):
  - It is observed experimentally that routing completion is often achieved using switch modules with $F_S = 3$ [Rose & Brown '91].
  - The switch modules used in Xilinx XC4000 have $F_S = 3$.
  - It is proved that a universal switch module can be constructed with $F_S = 3$ [Chang, Wong, Wong '96].

- Six types of connections:



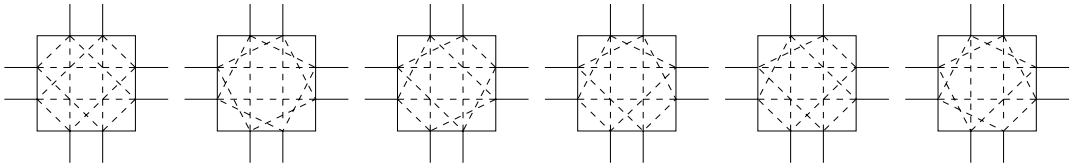
- *Routing requirement vector* (*RRV*): $\vec{n} = (n_1, n_2, \ldots, n_6)$, where n_i is the number of type-i nets.



(0,1,1,0,1,0) is routable but (2,0,0,0,0,0) is not with the above switch module.

- It is desirable to design a switch module with maximum # of routable RRVs.

Effect of Switch-Module Topologies on Routing



(a) S1 (b) S2 (c) S3 (d) S4 (e) S5 (f) S6

- Feasibility of routing (◯: routable; ×:unroutable)

RRV	S_1	S_2	S_3	S_4	S_5	S_6
$(1,1,1,0,1,0)$	◯	◯	◯	×	×	×
$(1,1,0,1,0,1)$	◯	◯	◯	×	◯	◯
$(1,0,1,1,0,0)$	◯	◯	×	◯	×	◯
$(1,0,0,0,1,1)$	◯	◯	×	◯	◯	×
$(0,1,1,0,0,1)$	◯	◯	×	×	×	◯
$(0,1,0,1,1,0)$	◯	◯	×	×	◯	×
$(0,0,1,1,1,1)$	◯	◯	◯	◯	×	×
# other routable RRVs	49	49	49	49	49	49
# routable RRVs	56	56	52	52	52	52

- S_1: Symmetric switch module; S_3: Xilinx XC4000-type switch module.

Universal Switch Module

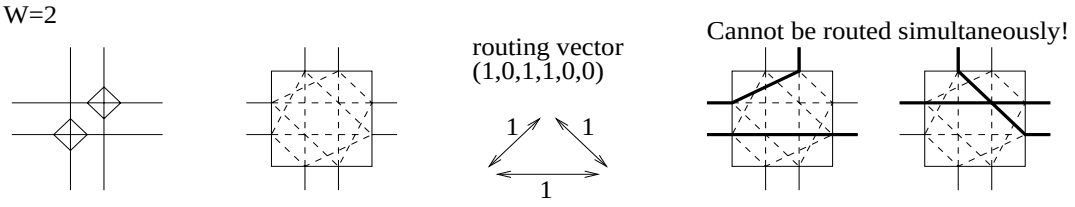
- A switch module S of size W is called *universal* if the following inequalities are the necessary and sufficient conditions for an RRV $\vec{n} = (n_1, \ldots, n_6)$ to be routable on S:

$$\begin{cases} n_1 + n_3 + n_6 \leq W \\ n_2 + n_3 + n_4 \leq W \\ n_1 + n_4 + n_5 \leq W \\ n_2 + n_5 + n_6 \leq W. \end{cases}$$

- A universal switch module has the maximum routing capacity (# of routable RRVs).
- A universal switch module with the minimum # of switches is of interest.

A Well-Known Switch Module

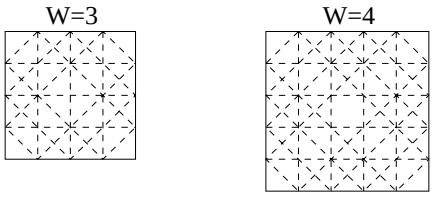
- Xilinx XC4000-type switch module ($F_S = 3$)



- It is not universal!
- Question: Does there exist a *universal* switch module with $F_S = 3$?

Design of Universal Switch Module

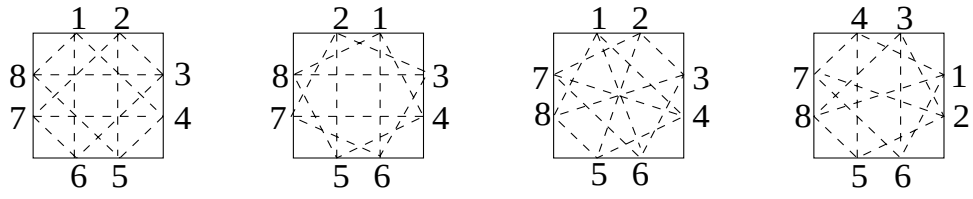
- Symmetric switch modules:



- **Theorem:** The symmetric switch modules are universal.
- The symmetric switch module with W terminals on each side contains $6W$ switches.
- **Theorem:** No switch module of size W with less than $6W$ switches can be universal.
- Question: Any other universal switch module with $F_S = 3$?

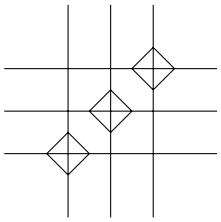
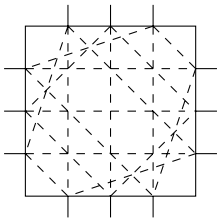
Other Universal Switch Modules

- Pin permutations induce isomorphic switch modules.



- **Theorem:** Any two isomorphic switch modules have the same routing capacity.
- All switch modules isomorphic to the symmetric switch module are universal.

XC4000-Type Switch Modules

(a)  (b) 

- **Theorem:** For an XC4000-type switch module S of size W, $\vec{n}$ is routable on S if and only if $\max\{n_1, n_2\} + \max\{n_3, n_5\} + \max\{n_4, n_6\} \leq W$.

Routing Capacity

- XC4000 switch modules
  - Feasibility condition:
    $X_W = \{\vec{n} | \max\{n_1, n_2\} + \max\{n_3, n_5\} + \max\{n_4, n_6\} \leq W\}$.
  - Routing capacity:
    $|X_W| = C_6^{W+6} + 3C_6^{W+5} + 3C_6^{W+4} + C_6^{W+3}$.
- Universal switch modules
  - Feasibility condition:
    $U_W = \{\vec{n} | n_1 + n_3 + n_6 \leq W,\ n_2 + n_3 + n_4 \leq W,\ n_1 + n_4 + n_5 \leq W,\ n_2 + n_5 + n_6 \leq W\}$.
  - Routing capacity:
    $|U_W| = \lfloor \frac{1}{6!}(10W^6 + 120W^5 + 595W^4 + 1560W^3 + 2320W^2 + 1920W + 720) \rfloor$.
- **Theorem:** $\lim_{W \to \infty} |U_W| / |X_W| = 1.25$.

Routing-Capacity Comparison

- Routing capacities:

W	Routing capacity: Universal $\lvert U_W \rvert$	Routing capacity: XC4000 $\lvert X_W \rvert$	Capacity ratio $\lvert U_W \rvert / \lvert X_W \rvert$
2	56	52	1.077
4	641	553	1.159
6	3,616	3,024	1.196
8	13,825	11,385	1.214
10	41,336	33,748	1.225
15	334,680	270,504	1.237
20	1,573,121	1,266,265	1.242
25	5,377,190	4,319,406	1.245
30	14,905,856	11,959,552	1.246

Experimental Results

- # Tracks needed for CGE detailed-routing completion:

Circuit	# Logic modules	# Connections	# Tracks (W): Universal	# Tracks (W): XC4000
BNRE	22×21	1257	12	14
BUSC	13×12	392	10	11
DFSM	23×22	1422	11	12
DMA	18×16	771	11	12
Z03	27×26	2135	14	15
Total			58	64