Examples of FPLD Families:

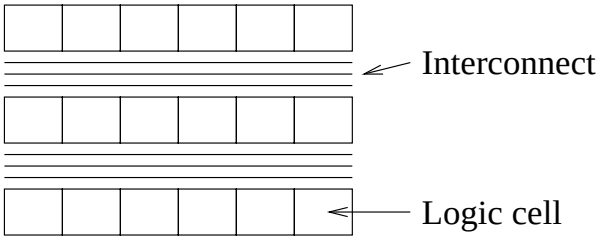
Actel ACT,

Xilinx LCA,

Altera MAX 5000 & 7000

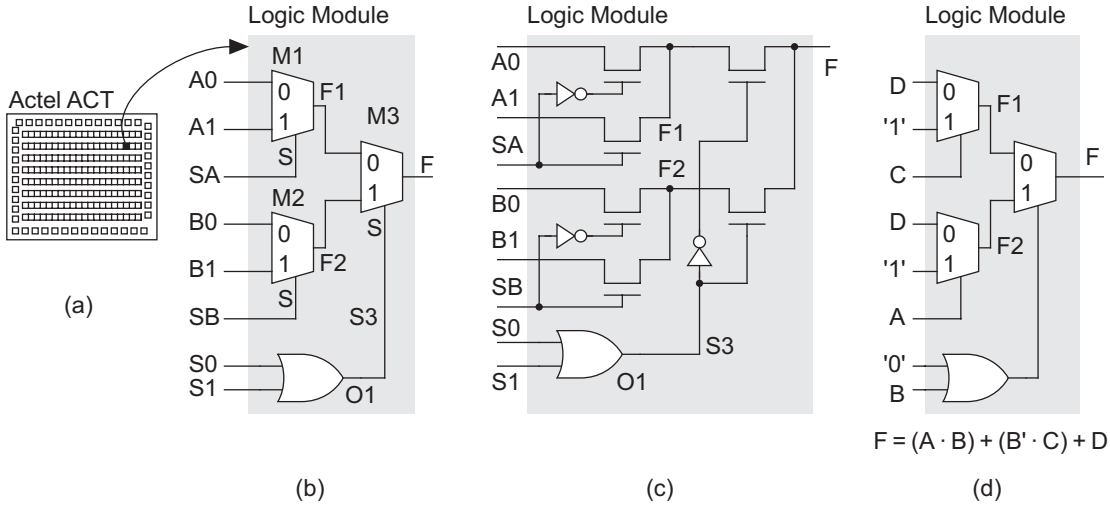
Actel ACT Family

- The Actel ACT family employs multiplexer-based logic cells.
- A row-based architecture is used in which the logic cells are arranged in rows with horizontal routing channels between adjacent rows of logic cells.



ACT 1 Logic Modules

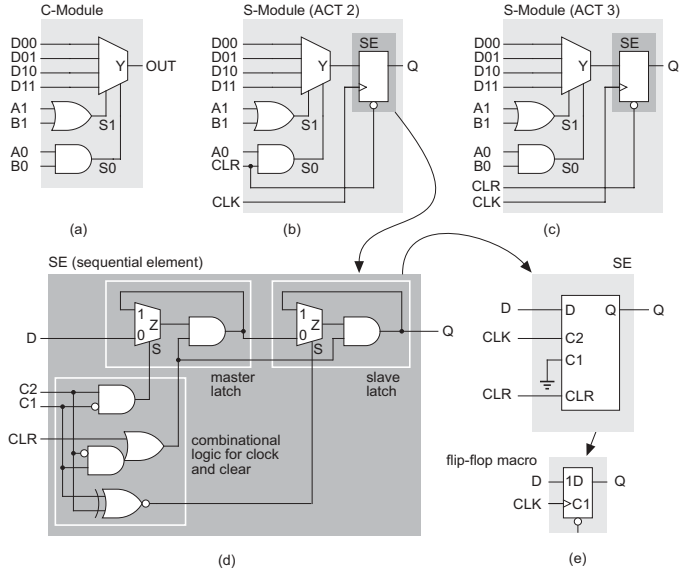
- ACT 1 FPGAs use a single type of logic module.



(a) An Actel FPGA. (b) An ACT 1 logic module. (c) An implementation of an ACT 1 logic module using pass transistors. (d) An example of function implementation by an ACT 1 logic module.

ACT 2 and ACT 3 Logic Modules

- Both ACT 2 and ACT 3 FPGAs use two types of logic module.

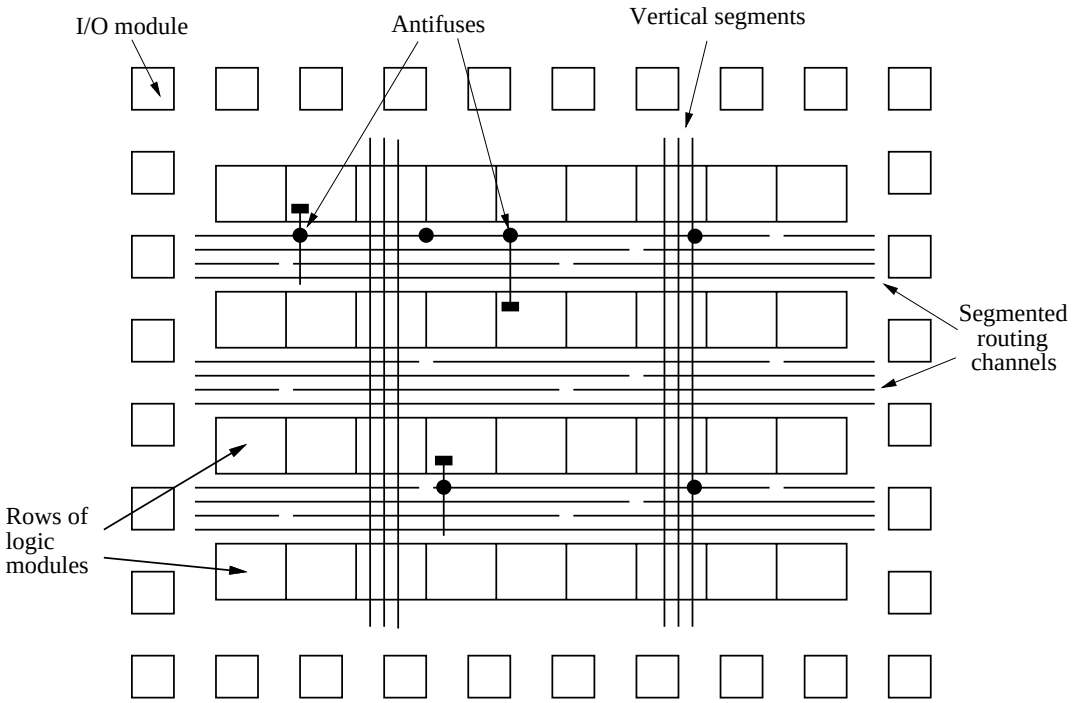


(a) The C-module used by both ACT 2 and ACT 3 FPGAs. (b) The ACT 2 S-module. (c) The ACT 3 S-module. (d) Equivalent circuit of the SE. (e) The sequential element configured as a positive-edge-triggered D flip-flops.

Routing Architecture of ACT Family

- A row-based architecture.
- Each horizontal channel consists of a number of routing tracks.
- Some routing tracks are segmented where adjacent segments can be connected through antifuses to form longer lines.
- There are also some vertical tracks running through the logic modules and horizontal channels.

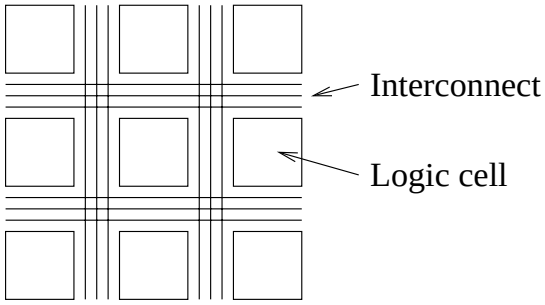
FILENAME.APP=6822FG13.PS



Routing architecture of an Actel ACT FPGA.

Xilinx LCA Family

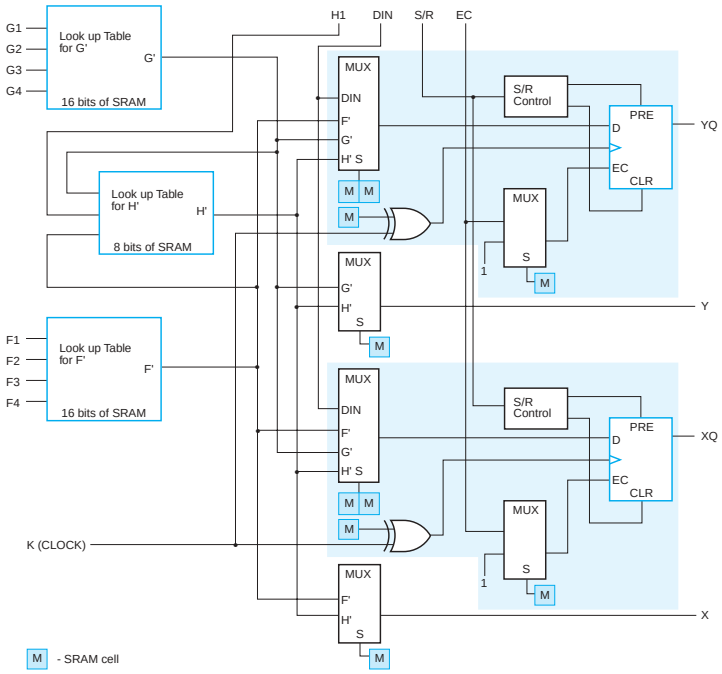
- The Xilinx LCA family employs LUT-based logic cells.
- A symmetrical array architecture is used.



Configurable Logic Block of LCA Family

- We consider the XC4000 devices for an example.
- The XC4000 FPGAs use a single type of configurable logic block (CLB).
- Each CLB contains two 4-input LUTs that feed a 3-input LUT. This allows a CLB to implement any two logic functions with four or less variables, or some function with five or more variables.
- A CLB can also be configured to be used as memory e.g. as two 16×1 memory SRAMs.
- The outputs of the function generators can be optionally stored in flip-flops inside a CLB.

6-37 Figure 6-32 Simplified Diagram of a Xilinx® Configurable Logic Block (Adapted with permission of Xilinx®, Inc.)



9

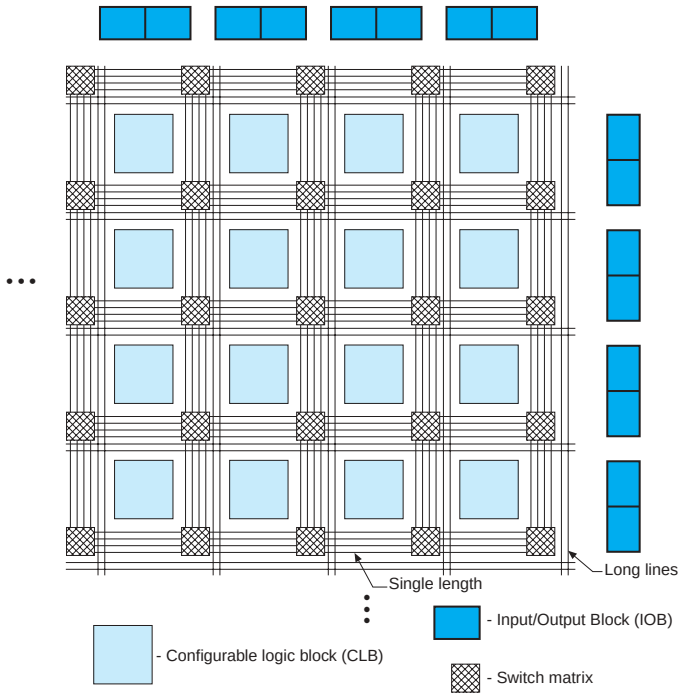
Routing Architecture of LCA Family

- A typical Xilinx LCA FPGA consists of a two-dimensional array of CLBs with horizontal routing channels between rows of blocks and vertical routing channels between columns.

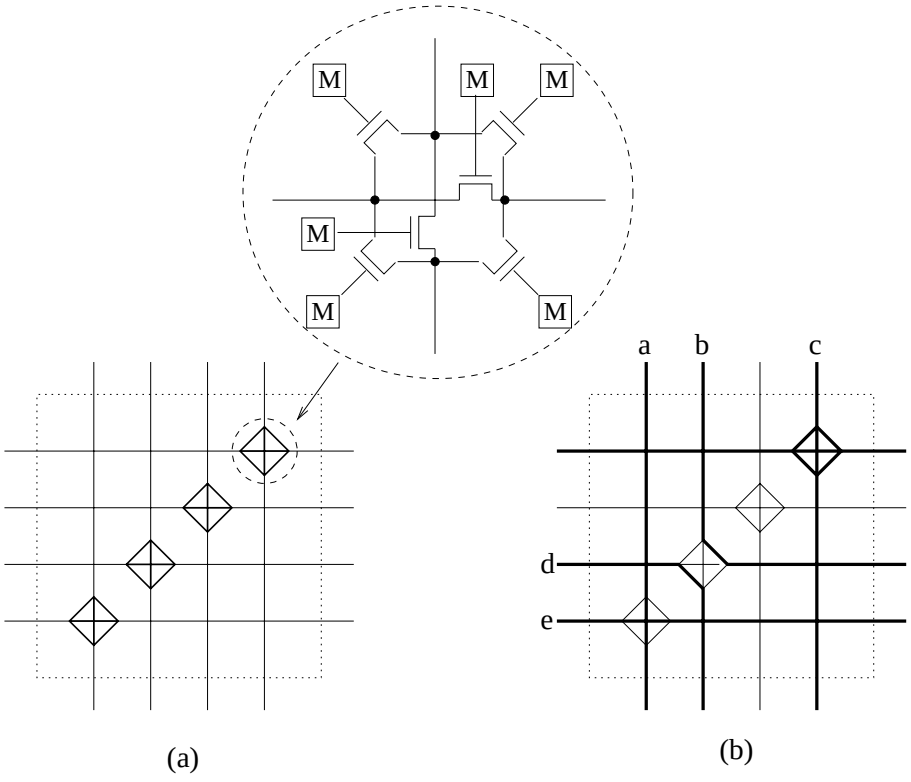
- Routing tracks are segmented which can be interconnected inside the *switch matrices*.

- Each interconnect point inside a switch matrix is formed by 6 pass transistors to allow connections between adjacent segments and/or between the vertical and horizontal lines that meet there.

T-153 **Xilinx® XC4000™ FPGA Structure (Adapted with Permission of Xilinx, Inc.)**



11

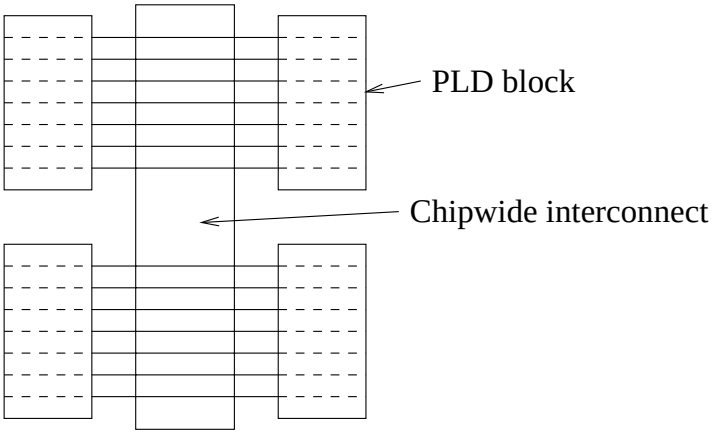


(a) A switch matrix. (b) Example of connections made through a switch matrix.

12

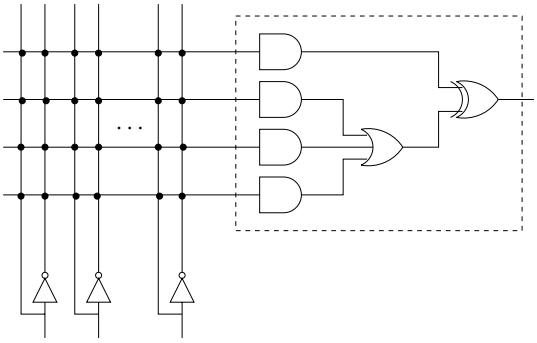
Altera MAX 5000 & 7000 Family

- The Altera MAX family employs PAL-based logic cells.
- The logic cells are called *macrocells*.
- A hierarchical PLD architecture is used where the macrocells are grouped into larger blocks called *logic array blocks*.



Logic Array Block of MAX Family

- Each logic array block (LAB) contains 16 macrocells.
- A simplified macrocell showing its basic PLD-like combinational logic structure:

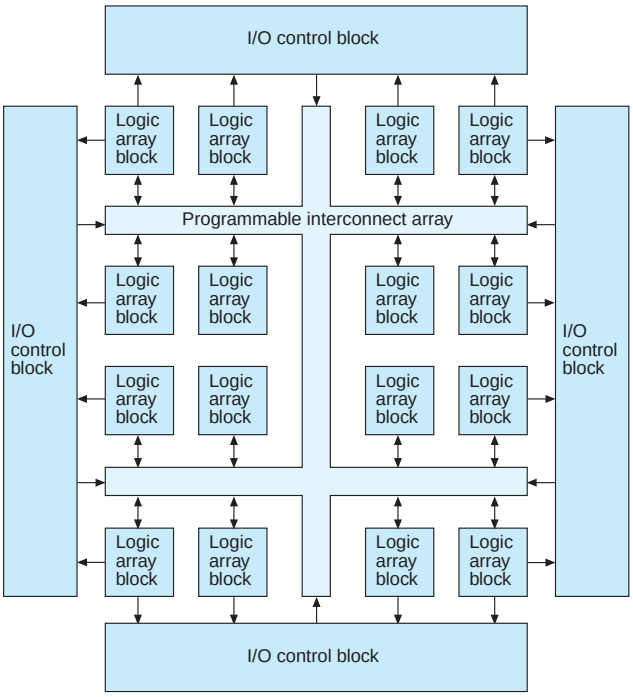


- See Fig. 3.5 of text for the complete structure of a macrocell.
- In addition to the basic combinational logic structure shown above
  – each macrocell has a flip-flop
  – there are special connections that allow sharing of product terms between different macrocells in the same LAB.

Routing Architecture of MAX 5000 & 7000 Family

- The LABs are interconnected by a chipwide interconnect called *programmable interconnect array (PIA)*.
- The PIA acts as a global bus and is built such that the connections between different pairs of LABs all have the same delay.

T-150 **Altera® MAX 7000™ Structure (Reprinted with Permission of Altera Corporation,© Altera Corp., 1991)**



Comparison of FPLD Families

	Actel ACT 3	**Xilinx XC4000**	**Altera MAX 7000**
Programming technology	antifuse	SRAM	EPROM
Architecture	row-based	symmetrical array	hierarchical-PLD
Logic cell type	multiplexer-based	LUT-based	PAL-based
Interconnect	segmented channels	segmented channels with switch matrices	programmable interconnection architecture
Interconnect delay	variable	variable	fixed
Basic logic cells	C-module and S-module	Configurable Logic Block (CLB)	16 macrocells in a LAB
Logic cell contents	C-module: 4:1 MUX, 2-input OR, 2-input AND. S-module: 4:1 MUX, 2-input OR, 2-input AND, latch/D flip-flop.	3 LUTs, 2 D flip-flops, 10 MUXes.	Macrocell: 5 ANDs, 1 OR, 1 EXOR, 1 flip-flop, 3 MUXes.
Combinational functions per logic cell	One. Most 3-and 4-input functions.	Two or one. Any two 4-input functions, or one selected function of $<=$ 9 inputs.	Multiple wide input functions per LAB
Basic logic cells per chip	104 S+96 C (A1415) to 697 S+680 C (A14100)	64 CLBs (XC4002XL) to 3136 CLBs (XC4085XL)	32 macrocells (EPM7032) to 256 macrocells (EPM70256E)