Programming Technologies and Architectures of FPLDs

Programmable Switches

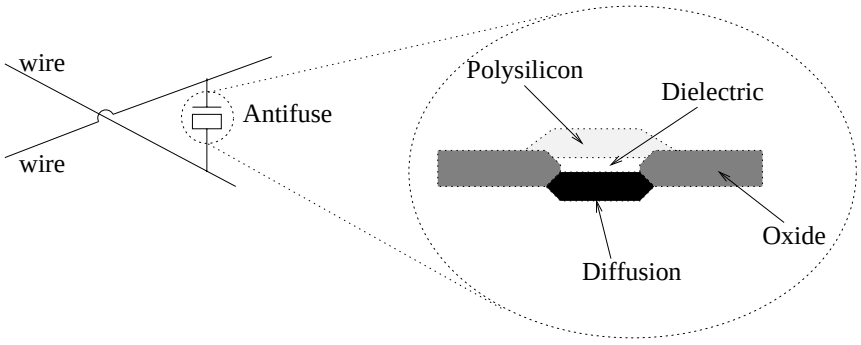
- Programmable switches are used for connections of wire segments in a FPLD.
- A FPLD may contain hundreds of thousands programmable switches.
- So they should
  – consume as little chip area as possible
  – have low ON resistance and very high OFF resistance
  – contribute low parasitic capacitance
  – be fabricatable in a large number reliably.

Programming Technologies

- Programming technologies may be permanent or non-permanent.
- For commerical FPGAs, the main switch technologies are *antifuses* (e.g. Actel) and *Static RAM cells* (e.g. Xilinx).
- For commerical CPLDs (e.g. Altera MAX), the main switch technologies are *Erasable Programmable ROM (EPROM) transistors* and *Electrically Erasable PROM (EEPROM) transistors*.

Antifuse Programming Technology

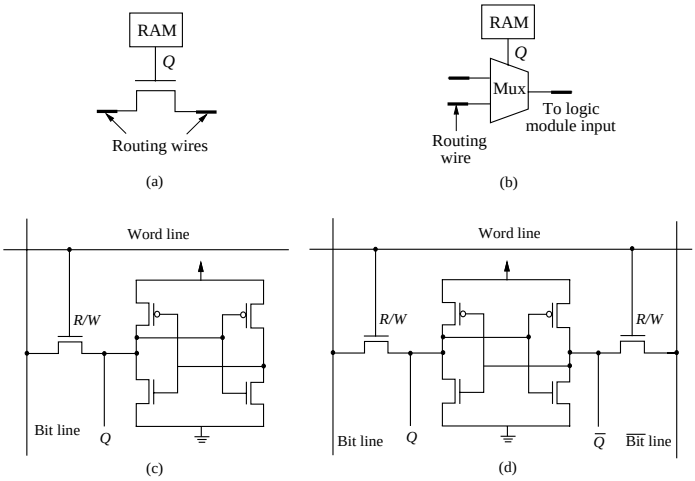
- An *antifuse* is the opposite of a regular fuse. It is an open path until a programming current is forced through it by applying a high programming voltage across it.
- Advantage: small (allow denser switch population).
- Disadvantage: only one-time programmable.



Actel's PLICE antifuse structure.

Static RAM (SRAM) Programming Technology

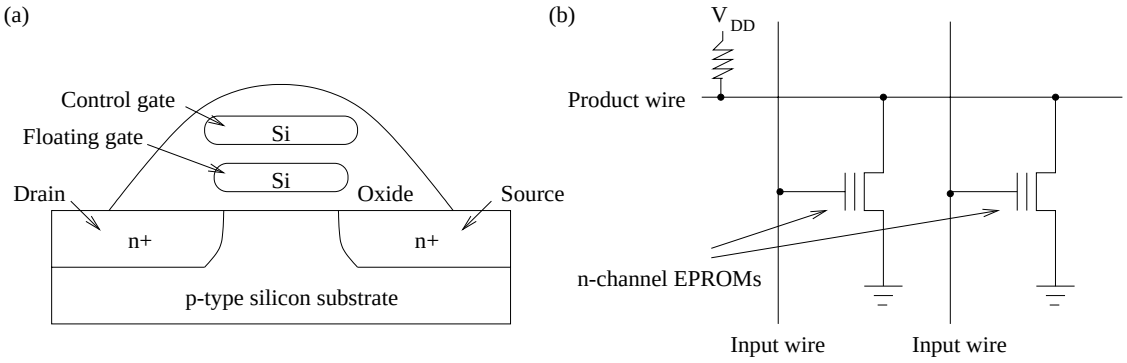
- Use SRAM cells to control pass transistors or multiplexers by the bit-content in the SRAM cells.
- Advantage: reprogrammable; Disadvantage: occupy more space.



(a)(b) A pass-transistor switch/multiplexer switch controlled by a RAM cell. (c)(d) SRAM cells implemented using five/six transistors.

EPROM Programming Technology

- Use an EPROM transistor as a programmable switch.
- A n-channel EPROM transistor is programmed by applying higher-than-operation voltages to the drain and the control gate.
- Become an open path when programmed because electrons trapped on the floating gate raise the threshold voltage of the n-channel EPROM transistor above V_{DD}.
- Erasable by exposing the floating gate to UV light.



(a) A n-channel EPROM transistor. (b) A section of an EPROM-based device.

Programming Technologies Summary

Programming technology	SRAM	Poly-Diffusion antifuse	Metal-Metal antifuse	EPROM	EEPROM
Manufacturing Complexity	$+$	$-$	$-$	$-$	$--$
Reprogrammable?	Yes In circuit	No	No	Yes Out of circuit	Yes In circuit
Physical size	Large (12X)	Small (2X)	Small (1X)	Small	Small
ON resistance (Ω)	600–800	100–500	30–80	1-4K	1-4K
OFF capacitance (fF)	10–50	3–5	1	10–50	10–50
Power consumption	$++$	$+$	$+$	$-$	$-$
Volatile?	Yes	No	No	No	No

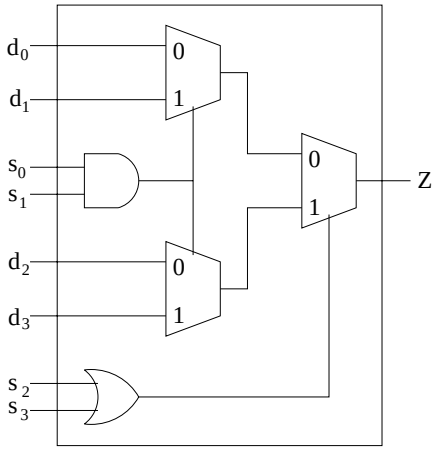
$+$ desirable; $-$ undesirable

Logic Cell Architecture

- Both FPGA and CPLD are made up of a set of basic logic cells.
- A basic logic cell has a fixed number of inputs and outputs, and can implement a certain set of functions.
- Logic cells used in FPGAs:
  – multiplexer based (e.g. Actel)
  – lookup-table based (e.g. Xilinx, Lucent)
- Logic cells used in CPLDs:
  – programmable array logic (PAL) based (e.g. Altera MAX, Xilinx XC9500).

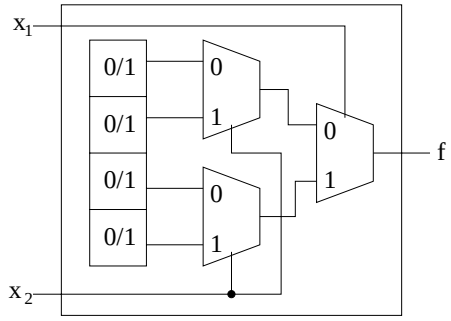
Multiplexer Based Logic Cells

- A multiplexer-based logic module is typically composed of a tree of 2-to-1 MUXes
- Below is an Actel ACT 3 C-Module. It can realize a wide range of different functions of up to 8 variables.
- Flip-flop can be incorporated into a logic cell to implement sequential logic.

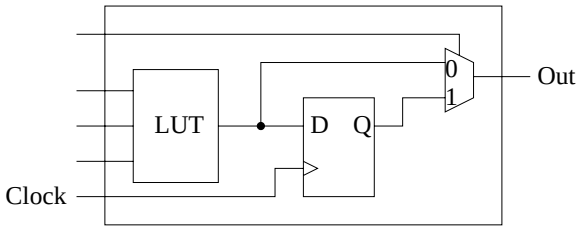


Lookup-Table Based Logic Cells

- A *lookup-table (LUT)* is a segment of SRAM e.g. a 5-input LUT is a 32-bit SRAM.
- Any functions of up to K variables can be implemented by a K-input LUT.
- Flip-flop can be incorporated into a LUT-based logic cell to implement sequential logic.
- A *coarse-grained* logic cell (c.f. *fine-grained* logic cell) typically contains several LUTs, multiplexers, and flip-flops.



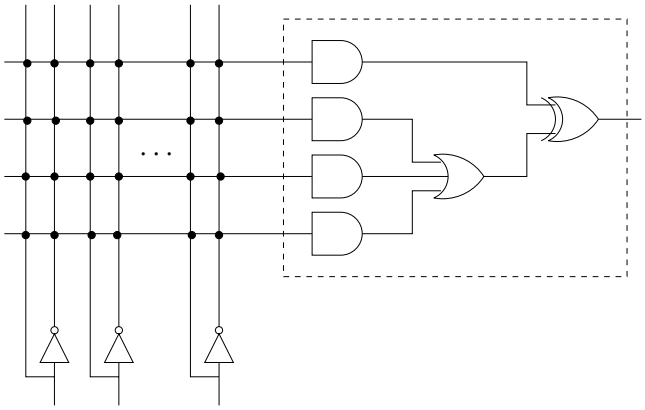
A 2-input LUT



A fine-grained logic block with a flip-flop.

PAL-Based Logic Cells

- CPLD uses logic cells evolved from a PAL-based architecture.
- A PAL based logic cell consists of wide fan-in (20 to over 100 inputs) AND gates feeding into an OR gate.
- Flip-flop can be incorporated into a logic cell to implement sequential logic.



The Altera 5000 series macrocell (simplified).

FPLD Routing Architecture

- The routing architecture determines the way in which programmable switches and wiring segments are positioned.
- Two issues: *routability* and speed.
- Routability – capability of an FPLD to accomodate all nets of a typical design.
- Speed – keep propagation delay low.