## Full-Custom ICs

- Design a chip from scratch.
- Engineers design some or all of the logic cells, circuits, and the chip layout specifically for a full-custom IC.
- Custom mask layers are created in order to fabricate a full-custom IC.
- Advantages: complete flexibility, high degree of optimization in performance and area.
- Disadvantages: large amount of design effort, expensive.

### Standard-Cell-Based ICs

- Use predesigned, pretested and precharacterized logic cells from standard-cell library as building blocks.
- The chip layout (defining the location of the building blocks and wiring between them) is customized.
- As in full-custom design, all mask layers need to be customized to fabricate a new chip.
- Advantages: save design time and money, reduce risk compared to full-custom design.
- Disadvantages: still incurs high non-recurring-engineering (NRE) cost and long manufacture time.

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Cell A	Cell B	
Cell C	Cell D	Feedthrough Cell

Standard-cell-based IC design.

## Gate-Array

- Parts of the chip are pre-fabricated, and other parts are custom fabricated for a particular customer's circuit.
- Idential base cells are pre-fabricated in the form of a 2-D array on a gate-array (this partially finished chip is called gate-array *template*).
- The wires between the transistors inside the cells and between the cells are custom fabricated for each customer.
- Custom masks are made for the wiring only.
- Advantages: cost saving (fabrication cost of a large number of identical template wafers is amortized over different customers), shorter manufacture lead time.
- Disadvantages: performance not as good as full-custom or standard-cell-based ICs.

- Channeled Gate Array vs. Channelless Gate Array (Sea-of-gates Array).
  - In channeled gate arrays, empty spaces are set aside between the base cells to accommodate the wires that will be added later to connect the cells.
  - In sea-of-gates arrays, there are no predefined areas set aside for routing between the cells, and the interconnection wires are fabricated on top of the cells.



Channeled Gate Array



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### Programmable Logic Devices (PLDs)

- A PLD is a general-purpose chip for implementing logic circuitry.
- Transistors and wires are already prefabricated on a PLD.
- Logic cells and interconnect can be programmed by end-user to implement specific circuitry.
- No need to create custom masks for each customer.
- Advantages: low non-recurring-engineering cost (ideal for low-volume production), fast turnaround time.
- Disadvantages: lower performance and larger chip size.
- Depending on capacity, complexity and architecture, may be further classified as (1) Simple PLDs (SPLDs),
  - (2) Complex PLDs (CPLDs), and
  - (3) Field-Programmable Gate Arrays (FPGAs).

	Full-Custom ICs	Cell-based ICs	Gate Arrays	High-Density PLDs
Speed	+++	++	+	—
Integration Density	+++	++	+	
High-Volume Device cost	++	++	+	+
Low-Volume Device cost			+	+++
Custom Mask Layers	All	All	Some	None
Fabrication Time			—	+ + +
Time to Market			++	+ + +
Risk Reduction			—	+ + +
Future Design Modification			—	+++
Educational Purpose				+++

## Comparison of Design Styles

+ desirable; - not desirable

# Growth Rate of the PLD Industry

Company/Industry	Annual Growth Rate in Sales		
	(1994 to 1998)		
Semiconductor Industry	27.78%		
Altera (a leading PLD provider)	36.07%		
Intel (leading microprocessor company)	24.50%		
LSI Logic (a leading ASIC provider)	15.71%		

## Programmable Logic Array (PLA)

- Classified as a simple programmable logic device (SPLD).
- The first programmable logic device introduced in the early 1970s by Philips.
- Based on the idea that logic functions can be realized in sum-of-products form.
- A programmable AND array followed by a programmable OR array.

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T-146 PLA with Three Inputs, Four Product Terms, and Two Outputs



#### Programmable Array Logic Device (PAL)

- A device similar to PLA.
- Introduced to overcome the weaknesses of PLAs at that time (programmable switches were hard to fabricate correctly and introduced significant propagation delays) by MMI.
- A programmable AND array followed by a fixed OR array.
- PAL usually contains flip-flops connected to the OR gate outputs to implement sequential circuits. The term *macrocell* is used to refer to an OR gate combined with a flip-flop and extra circuitry in a PAL.

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T-148 PAL® device with Four Inputs, Four Outputs, and a Three-wide AND-OR Structure

1997 by Prentice-Hall, Inc.



Structure of a macrocell.

## Complex Programmable Logic Device (CPLD)

- A CPLD comprises multiple PAL-like blocks on a single chip with programmable wiring to connect the blocks.
- Each PAL-like block consists of a number of macrocells.



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### Field-Programmable Gate Array (FPGA)

- FPGA is a high capacity programmable logic device.
- A FPGA consists of an array of programmable basic logic cells surrounded by programmable interconnect.
- Introduced in 1985 by Xilinx.
- Can be configured/programmed by end-users (*field-programmable*) to implement specific circuitry.
- Can implement combinational and sequential logic.
- Capacity: 1K to 1M logic gates.
- Speed: up to 100MHz.
- Popular applications: prototyping, FPGA-based computers, on-site hardware reconfiguration, DSP, logic emulation, network components, etc.

