ECE 480a Lab 1
VHDL Concepts

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Chapter 1

Theory and Background Information (2 marks)

Simulations play very important part in system design...

1.1 VHDL

VHDL is a powerful simulation language...

1.2 SYNOPSYS

The Synopsys software package allows the engineer to ...

1.3 Lab Objectives

The lab experiments and analysis will provide the basis for ...

Chapter 2

Experiment

2.1 Part 1: Software

2.1.1 Software Configuration (1 mark)

The experiments were be performed on using the following software...

2.1.2 Synopsys (1 mark)

Synopsys ver: has been configured to run under Solaris ver:..

2.2 Part 2: Simulations

Two logic circuits were analyzed..

2.2.1 Simulation of the VHDL model (1 mark)

The vhdldbx tool has been used to simulate and analyze the VHDL models of...

AND Gate (1 mark)

VHDL code of a two input AND gate:

Full Adder (1 mark)

....

2.3 Part 3: Design Analyzer

The analysis of the gate designs were conducted using...

```
--------------------------------------------------------------------------
-- Two-input AND gate
--------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;
entity and2_gate is
    port (in_1    : in std_logic;
          in_2    : in std_logic;
          output : out std_logic);
end and2_gate;


-- structural description of adder using component instantiation statements
library work;
architecture structural of and2_gate is
 begin
 output <= in_1 AND in_2;
end structural;
```

Figure 2.1: VHLD Listing of an AND Gate

design: and2_gate	designer:	date: 10/30/2002
technology: gtech	company:	sheet: 1 of 1

Figure 2.2: AND Gate

2.3.1 Hierarchy Design (1 mark)

2.3.2 Logic Synthesis (1 mark)

Chapter 3

Discussion

3.1 Results (1 mark)

The Synopsys software has been used to obtain the following results...

3.2 Summary (1 mark)

3.3 Conclusions (1 mark)

Bibliography

[1] W. Wang, *ECE 480a Laboratory Manual*, UWO, 2002

[2] Author *Title*, Publisher, Year of publication