OPEN SYSTEMS RELAYING


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Abstract

This paper describes a development in relaying hardware and philosophy which has been made possible by DSP's and industrial grade pc's. Details are given of a prototype design capable of being assembled and configured by a Utility and results of tests on this prototype using the RTDS at the Manitoba HVDC Research Centre are presented. The project is a joint effort between the University of Manitoba and Manitoba Hydro.

Keywords. Programmable Digital Relays, DSP, C.

INTRODUCTION

The utilisation of the early 8 and 16 bit microprocessors to implement relay functions required specialists in the machine code of the particular microprocessor employed in the design. Integer arithmetic was all the CPU could manage and certain arithmetic procedures such as a divide were out of the question due to the time such a routine would take. Fourier based impedance relays [1] [2] could just about manage a DFT based on 8 to 12 samples a cycle to calculate the fundamental V and I phasors in \( a + jb \) form but had no time left to calculate \( \sqrt{a^2 + b^2} \) (another time consuming operation) far less perform \( \sqrt{V} \) to find the impedance. Numerous clever algorithms based on the real and imaginary parts of the V and I phasors were utilised to arrive at impedance loci of suitable shapes. Like the analogue relays they were replacing they implemented an operate region without calculating where in the operate region the impedance lay. If this was required for say fault location then it could be computed at leisure after the protection decision had been taken. This was a very useful feature but could not be implemented on-line in the time available. Furthermore to develop a microprocessor board type relay required expensive tools such as an "In Circuit Emulator" which plugged into the board via an umbilical cord type connection to replace the microprocessor while the program to run the microprocessor was being evolved.

There was no way that utility relay engineers could think about trying to develop their own relay and the task was left in the hands of the manufacturers as it had always been. Notwithstanding these points, the emerging digital technology brought new manufacturers on to the scene to increase the consumers choice of product.

Despite the greater choice of product there is an ever increasing number of Utility specific relaying problems which any one manufacturer's protection system cannot quite handle. The manufacturer can no doubt tailor the system to meet these needs but these will likely be a cost penalty and, perhaps more important, a time penalty. Furthermore there is increasing pressure to integrate the protection systems into the control and instrumentation arrangements. How is this to be achieved if you buy your relay from one manufacturer and your instrumentation/SCADA system from a different source?

In comparison to the change from electromagnetic to solid state analogue electronic devices the advances in digital technology are proceeding at a pace which is difficult for the majority of relay engineers to follow. These same advances however will give the relay engineer much greater choice in the design of future relays in which the detail of the digital hardware is transparent to the end user. This is the same situation as exists with regard to personal computers where a standard mass produced piece of hardware can perform a huge variety of tasks depending only on the software installed. Ease of use of the software depends on the interface and it will be no different with future relays. There are of course issues of the robustness of the software and the protection of hardware in a hostile electromagnetic environment but these are concerns for any industrial user of pc type equipment. Industrial grade pc's are available in the market place and are being incorporated in many vital control processes where integrity of performance is just as important as in relaying.

As always there are therefore developments taking place in fields outside relaying which will have a profound effect on the future of relaying. This paper attempts to show what can already be done by a Utility sympathetic to changes in relaying hardware and philosophy. Whether such changes gain widespread acceptance will depend on market forces but will also be dependent on an adequate supply of engineers with some knowledge of power systems and a familiarity with computers. The title of this paper has been drawn from terminology used in the energy management field where a plethora of manufacturer specific
equipment has led to difficulty in expanding the system without changing everything. Open Systems Energy Management philosophy demands that manufacturers provide equipment that can be expanded or changed by the Utility or another manufacturer. The type of relaying described in this paper is heading in the same direction with standard hardware which can be customised by the Utility, any manufacturer or specialist consultant, to meet the specific needs of a particular application.

The paper describes part of a joint project between the University of Manitoba and Manitoba Hydro which addresses some of the issues raised above. A group of projects funded by Manitoba Hydro has looked at particular relaying problems within the Manitoba Hydro system and the overall project has become known as the "Adaptive microprocessor protection systems" (Amps) project. All of the projects will use a generic piece of hardware capable of implementing all of the relaying functions but with the capability to expand as the need arises. It should also be configurable by the relay engineer without specialist computer knowledge and be capable of integration into the data acquisition/instrumentation scheme used by the Utility. It must also preserve the integrity of the relaying function in a typical substation environment.[3]

**BASIC DESIGN FEATURES**

The majority of protection functions are based on the fundamental power frequency components of fault waveforms. This is consistent with the operation of the older electromagnetic relays and the solid state relays which have replaced them. "Instantaneous" type relays such as current differential systems can also use the instantaneous value of the fundamental component phasor which is tantamount to using a bandpass Fourier filter centred on the fundamental frequency [4]. With this in mind it was decided to use a basic measuring system which would output the real and imaginary parts of the fundamental component and as many harmonics as were consistent with the sampling rate. This decision was made with the knowledge that there were numerous floating point Digital Signal Processors (DSP's) on the market custom built to implement the FFT algorithm. This algorithm requires that the number of samples per cycle is of the form $2^n$ eg 8, 16, 32 etc. The speed with which such processors can carry out a complex $(a + jb)$ type multiply frees the designer from any worries about the effect of the number of samples per cycle on the multiplying factors used in the Fourier algorithm. Because the Manitoba Hydro system contains a high capacity HVDC converter station it was felt that there may at some time be a need for harmonics in excess of the 7th. $2^5$ was therefore chosen as the number of samples per cycle giving up to the 15th harmonic on any input variable. If the sampling rate is fixed and the fundamental power frequency varies slightly say within $\pm 0.5\text{Hz}$ then the effect on the accuracy of the calculated amplitude and phase for the higher harmonics can be significant. Add to this the knowledge that if the device is to be used on the ac collector system on the Nelson river which feeds the HVDC system then the frequency can vary between 54 and 85Hz during sudden pick up or loss of a dc bipole. The sampling rate had to be adaptive to allow for this type of variation and a measure of frequency would be required anyway for under or over frequency applications.

If the measurements were to be of use in both protection and instrumentation applications then the dynamic range with acceptable accuracy for the current channels would need to be greater than afforded by a standard 12 bit A/D converter with a fixed gain input. If a variable gain amplifier is used as the interface between the signal and the A/D then information is lost during the period when a decision to change the gain is being implemented. To avoid this loss of information each ac current would have two input channels each continuously sampled and the software would decide which channel to use in the calculations.

When the relay issues a trip signal the waveforms on which that trip decision was based should be recorded for subsequent analysis. Some pre-fault information should be included with such recordings and the recording should be about 20 cycles in duration for each input channel. Recordings should also be available on demand to check operation. The relay would interface to the user via a serial port to a pc or workstation.

The final design constraint imposed at the outset of the project in the summer of 1989 was that the final hardware should not cost more than $1000 (Canadian).
The voltage and current signals would be taken through auxiliary CT's and PT's and suitably buffered and protected to avoid damage to the conditioning amplifiers connected to the A/D inputs. Such an interface unit had been developed for a disturbance recorder project and required only minor modification to suit this application. The unit had been fully tested to Utility grade levels and was already in use on disturbance recorders in the Manitoba Hydro system. Figure 1 shows the dual channel input for the current with a factor of $32$ difference in the gains. For the 5A secondary the $5V$ limit on the input to the amplifiers allows for a fully offset $100A$ rms current at the upper end down to $0.025A$ rms current with 5 bit or 5% accuracy. The lower limit in our case was set by the interference levels causing the next bit in the A/D to flicker. This level could be improved upon if the board housing the A/D's was not a wire wrapped prototype. Figure 2 shows the arrangement of the basic 9 input channels. Channel 1 is shown in detail and shows the anti-aliasing filter with an adjustable bandwidth set by the present frequency value as calculated by the frequency tracking routine.

**Basic Software Description**

The basic sampling process is shown for a single variable in Figure 3. The process is described in terms of a typical three current and three voltage input for the protection of say a transmission line. The incoming samples are held in a buffer and when the FFT does a calculation for this channel it will select the 32 most recent samples in the buffer. The FFT routine performs all variables and the various calculations which depend on the output from the FFT eg rms values, relay functions etc are performed in between the sampling instants. To complete a full set of calculations may take more than one sampling instant but all that then happens is that the sampling process continues into the buffer and when the processor is ready for the next set of calculations it takes in the 32 most recent samples. Timing for a full set of calculations is given in a later section with regard to a particular relay.

As explained earlier it is essential that the sampling interval is dynamically altered to maintain 32 samples per power system cycle. There are numerous techniques available to track the frequency but the technique used here is to calculate the positive sequence voltage phasor from the fundamental voltage phasors for the phase voltages. The angle of this phasor is then compared to a reference position which rotates at the set frequency. If the frequency remains constant then the positive sequence phasor is in phase with the reference position and no correction is needed. If the phase difference exceeds say $6^\circ$ then a correction is made to the frequency according to the equation

\[ F_s = F_s + \Delta F_s \]  

where

\[ \Delta F_s = \pm 32 \times F_s \frac{5}{2\pi k} \]
that the first prototype was developed into a very powerful relay/recorder platform[3] in terms of what is currently commercially available, there turned out to be no reasonable way that a relay engineer without NEC programming expertise could configure the relay. A menu of available relay functions allowed a choice of functions but this menu could not be expanded without expert help. Much of the problem stemmed from the fact that there was no cross-assembler from a high level language such as C to the NEC machine code. Another potential problem was that the design required a special purpose board to be assembled which would require a manufacturing capability. Nonetheless the development did show the potential calculating power from a board using a state of the art floating point DSP.

Based on the lessons learned from the first prototype and taking advantage of a new DSP with a cross assembler from C a second prototype was commissioned. The earlier financial constraint was relaxed to allow the project to realise the goal of having a device which could be configured by a relay engineer and which would require a minimum of manufacturing capability. This design was based on a 386 motherboard combined with off-the-shelf plug in boards. One of these boards housed the DSP and had an interface which was completely compatible with the motherboard.

The signal being tracked is

$$F = 60 - 10\sin(t)$$ (3)

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$$\sin(2\pi \int Fdt) + 5\% \text{ random noise}$$ (4)

and is shown below the tracking graph. The maximum rate of change of frequency in equation (3) is 10Hz per second.

An alternative tracking algorithm checks the position of the positive sequence voltage phasor every 32 samples and compares the angle to the previous angle +2\pi. Any difference angle \(\delta\) is used to set the new sampling interval \(\Delta t'\) as in the following equation

$$\Delta t' = \Delta t \left[\frac{1}{1 + \delta/2\pi}\right]$$ (5)

Even under the extreme condition of frequency varying at a rate of 10Hz per second \(\delta\) is small enough to allow equation (5) to be expanded as a binomial expression and evaluated to sufficient accuracy using only three terms. This algorithm tracks the frequency more closely than the previous algorithm.

Before discussing the relay algorithms in detail it is necessary to consider the hardware to be used to implement the 9 channel FFT and the frequency tracking.

**HARDWARE CONFIGURATION**

The first prototype was wire wrapped in the summer of 1989 and was based on a NEC 77230 DSP and a Motorola 68000. An In Circuit Emulator was available for the NEC and the individual implementing the algorithms was an expert in NEC code. The financial constraint and the convenience of the NEC equipment and programming expertise led to a board level development. Despite the fact that the first prototype was developed into a very powerful relay/recorder platform[3] in terms of what is currently commercially available, there turned out to be no reasonable way that a relay engineer without NEC programming expertise could configure the relay. A menu of available relay functions allowed a choice of functions but this menu could not be expanded without expert help. Much of the problem stemmed from the fact that there was no cross-assembler from a high level language such as C to the NEC machine code. Another potential problem was that the design required a special purpose board to be assembled which would require a manufacturing capability. Nonetheless the development did show the potential calculating power from a board using a state of the art floating point DSP.

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The use of a DOS based motherboard capable of accepting other plug-in boards, and running a hard disk, opened up many other possible applications such as transient and disturbance recording with a modem for remote interrogation. The relay board can act as the computing "engine" for all the recording and instrumentation applications by downloading the waveforms and rms values to the motherboard either for storage or for slower applications such as instrumentation or disturbance recording. **All the relaying functions are carried out on the relay board and the relay board, once programmed, runs independently of the motherboard.** This allows the other functions such as the modem communications to operate in parallel with the relay and the motherboard can also be rebooted without in any way affecting the relay. In this sense the relay operates in exactly the same way as a single board unit connected to an external pc by a parallel port. The only difference is that the pc is permanently connected in this case.

Figure 5 shows the hardware configuration for the new platform. It consists of two separate "boxes" the second "box" enclosing the same interface unit as was used on the first prototype. Figure 6 shows the relay card in the motherboard enclosure with the DSP chip on the left hand side. The only part of the hardware which is not off-the-shelf is the A/D board and this is a relatively simple board to manufacture. The cost of the new hardware which is a 33MHz 386 including a graphics card to drive a super VGA monitor and a 100MB hard disk is approximately $8000. This includes the cost of the relay card which alone costs $4000.
Relay software

Although the algorithms for the DSP can be written in a high level language (C) we found it expedient to have an expert in the machine code for the new DSP optimise the code for all the core calculations eg FFT, rms values, sequence components, frequency tracking, ground and phase impedances etc. This is a common problem with general purpose cross assemblers. The optimised code was then embedded in subroutines called from C. While we have not entirely succeeded in having the relay engineer program the DSP they can make up new functions based on the coded routines. They will have to be able to write simple C code eg to set up a quadrilateral impedance zone for the phase "a" ground fault relay requires two lines of code

\[ \text{CreateRegion}(\&GndTrip, 4, -1, 0, 0, 3, 2, 3, 1, 0); \]  
\[ \text{TripAN} = \text{Inside}(\&GndTrip, \&Zan); \]  

The CreateRegion and Inside subroutines are C subroutines and Zan is one of the core routine outputs. Statement (6) creates a 4 vertex figure with the x,y coordinates for the four vertices as given. Statement (7) checks if the given impedance is inside the defined region. Even this simple procedure has been improved upon to allow the engineer to construct the shape of any particular zone using a graphics routine whereby the vertices of the trip region are defined either by clicking a mouse or, to get exact values entered for x and y, by filling in a box at the top right of the screen. Figure 7 shows the screen during such a process. The graphics image is then translated into the code to be downloaded to the DSP without any need for...
Figure 8: Recordings taken by the relay for a 3-phase fault 50 per cent down the line

the engineer to write code. Not all of the relay functions have been put in this graphics form but the eventual aim is to have an Icon driven menu whereby the engineer can click the Icons for the desired functions, set the parameters in each function and then build a block diagram from the edited Icons to enforce the relay logic and timing.

**TEST RESULTS**

The application selected to test the relay platform was the protection of the 500kV line from the Dorsey Converter station in Manitoba to the Forbes substation in Minnesota. The case data for these tests were already available from site tests on the 500kV line relays and were therefore simple to set up on the RTDS [5] at the Manitoba HVDC Research Centre. The relay platform was programmed to implement the significant features of both of the existing relays on the line plus a transient data recording facility. The functions are listed below and will be shown in greater detail on the recordings.

- High set positive sequence overcurrent \(|I_1| > 9A\) (secondary level); Direct trip and transfer trip.
- Biassed zero sequence overcurrent \(|3I_0| - K_0 |I_1| > 5A, K_0 = 0.1\); Direct trip and transfer trip.
- Negative sequence directional and overcurrent \(-180 < \Phi_2 < -20\) and \(|I_2| - K_2 |I_1| > 0.5A\) with \(K_2 = 0.1\). Transmit unblocking carrier and allow local trip if incoming carrier present. Otherwise initiate local trip after 400ms.
- Three phase-to-ground impedance elements with 2 zones, Zone 1 to give direct trip and Zone 2 to transmit permissive trip and local trip after 400ms.
- Three phase-to-phase impedance elements with 2 zones, logic as above.
- Record 300ms of all input variables for any of the above with some pretrip cycles.

The program to implement all of these functions is written in C and translated to machine code for the DSP by a compiler on the motherboard. It is downloaded to the relay board by calling a command routine and the transfer takes less than 1ms.

Tests were conducted on the programmed relay to find out how long it took to complete a full set of core calculations (FFT, rms, etc) and complete the above relay algorithms. This figure turned out to be 1.4 sampling intervals. All values will therefore be updated twice every three sampling intervals.

The relay was set at values consistent with the existing relays on the 500kV line and subjected to fault signals from the RTDS. Figure 8 shows the record displayed by the relay/recorder for a 3-phase fault within zone 1. In addition to the fault waveforms the dynamic impedance value for each of the measuring elements is superimposed on an impedance plane containing the set trip zones. Th-
time zero is set as the instant a trip was initiated. The trip could have been due to any of the impedance elements. To find out which element caused the trip the recording can be stepped through from the beginning and the dynamic Z plots will show which Z element enters a zone 1 first. The values of Z for the six measuring elements are calculated on-line by the relay board and used in the protection function. The actual display is in colour making it easier to distinguish the three phases from each other. In order to check the independence of the relay board from the motherboard faults were applied when the motherboard was being rebooted, while earlier recordings were being displayed, and while new settings were being configured but not downloaded. The relay operated correctly in all instances.

CONCLUSIONS

The present prototype platform has achieved most of the aims of making it possible for a utility with some assembly help from a local manufacturer or a relay manufacturer to configure their own relay/recorders. The capability of off-the-shelf computing hardware will make it possible to implement hitherto difficult relay algorithms (time consuming) thereby solving some difficult application problems. There is plenty of time for the platform to implement either more relay functions or to handle the protection functions for more than one line. The limitations are likely to be space for more input channels on the interface board.

The relay platform will be installed in the Dorsey 500kV substation and connected to the ct and cvt secondaries. In the first instance it will not be connected to the breaker but will act as a fault recorder in the event of a line fault: a transient recorder in the event of increased harmonic levels due to GIC; and it will run a loss of life calculation on the 500kV line transformers based on the voltage and current into the 500kV line. The latter algorithm is computed on the motherboard based on the rms quantities downloaded from the relay board. Instrumentation variables such as P, Q, V, I, Z, cos θ, and f (frequency) will be available on request. Protocols will be worked out for communication with the relay and how new relay or recording functions are to be loaded into the relay.

Whether utilities will take over the job of assembling and configuring their own relays or will choose to continue buying a ready made product from traditional suppliers remains to be seen. It is inevitable that the hardware costs quoted in this paper will decrease and for utilities with the appropriate manpower mix, configuring their own protection systems is a real possibility in the foreseeable future.

Acknowledgements

The authors wish to acknowledge the help of their colleagues on the Amps committee of Manitoba Hydro and the contribution of Mr. Yi Hu to the frequency tracking algorithm. The University authors wish to acknowledge the financial support of Manitoba Hydro and The National Science and Engineering Council of Canada.

References


BIOGRAPHIES

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Discussion

R. E. Wilson (University of Wyoming, Laramie, WY): The authors have produced an excellent paper on using an industrial grade personal computer (PC) as a relaying platform. The paper has a good balance between relaying science and concepts possibly less familiar to a practicing engineer, such as "C" language programming and digital signal processing (DSP) chips. The relay described has several nice features. The recording of voltages and currents when the relay assets a trip decision is a feature appreciated by system analysts.

In the section on "Test Results," the authors discuss the use of their Real Time Digital Simulator (RTDS) for relay testing. The use of laboratory equipment such as the RTDS (or equivalent) is an excellent way to verify relay performance. However, not every utility can afford this style of testing. A possible alternative would be the use of a manufacturer supplied relay macromodel for use in ElectroMagnetics Transients Program (EMTP) simulations. As the relaying community knows, there are several versions of EMTP. With a certified relay macromodel, relay engineers would simulate and verify measuring unit and relay logic performance with a PC on their desk for relatively low cost.

The authors state that their relay software was developed in the "C" language. Recent work has produced an EMTP-TACS-FORTRAN interface [1, 2]. Would the authors please comment on:

1. The availability of a relay macromodel,
2. The availability of a relay macromodel written in FORTRAN.

Future relay algorithms may require time synchronized digital samples at all line terminals. Global synchronization can be done by using a Global Positioning System (GPS) or GPS-GLONASS receiver-clock (GLONASS is the Russian equivalent of GPS). Could a GPS receiver card (GPS engine) be added to the industrial PC mainframe? Could the analog-to-digital converters used in relay described in the paper be globally synchronized?

A related issue is frequency syntonization. In the Conclusion, the authors state that instrumentation variables such as F (frequency) are available. What is the reference for the relays measurement of frequency? When discussing the frequency tracking software, the authors state the angle of a positive sequence voltage phasor is compared to a reference which rotates at the set frequency. How is this set frequency determined? Is the set frequency compared with a national standard? Is frequency syntonization for this relay an issue?

Again, the authors are to be commended on writing an informative and well structured paper.

References


Manuscript received August 9, 1993.
The other two issues on GPS signals and frequency measurement are related to the design philosophy of the relay. It would certainly be possible to insert a GPS receiver card if a slot was available on the motherboard or backplane. On the other hand we would not wish to synchronize the A/D converter to a global reference since the timing of the sampling instants is part of the frequency tracking adjustment. Bearing in mind the wide frequency range the relay may have to cover it is essential that the sampling interval be kept at 1/2 of a power system period. Otherwise the FFT or DFT will not be accurate due to non-rejection of harmonics. The rotating reference phasor is a local variable based on the last correction to the sampling interval. If the angle of the positive sequence voltage is checked every 32nd sample using tan⁻¹ (Imag/Real) then the angle should be the same as it was 32 samples ago. Any difference is used to adjust the sampling interval unless the difference is greater than a set limit in which case the interval is locked at its previous value until the difference between two successive checks comes back within range. The frequency is calculated from the inverse of 32 x (the sampling interval) and will be dependent on the accuracy of the DSP clock.

The frequency measurement was intended for use in load shedding applications rather than in any system wide synchronization. The best which could be achieved in this respect with the present sampling philosophy would be to know the exact instant at which the positive sequence voltage was calculated and linearly extrapolate the phase to the instant required. The time difference over which the extrapolation was calculated would typically be no more than one sample interval since the value of the positive sequence voltage is calculated every one or two sampling intervals.

References


Manuscript received October 1, 1993.