

# Western University Faculty of Engineering Electrical and Computer Engineering Program

## ECE 2205 - Electric Circuits

# **Course Outline Fall/Winter 2025**

**COURSE DESCRIPTION:** This course introduces fundamental properties and methods for analysis of direct current (DC) electric circuits including components such as resistors, capacitors, inductors, operational amplifiers, switches, and ideal and dependent voltage and current sources. Both steady-state and transient circuit behaviour are covered as well as practical applications of circuit analysis.

## **ACADEMIC CALENDAR:**

https://www.westerncalendar.uwo.ca/Courses.cfm?CourseAcadCalendarID=MAIN 014970 1&S electedCalendar=Live&ArchiveID=

Basic resistive circuits, Ohm's, Kirchhoff's Laws. DC analyis: nodal and mesh analysis. Network theorems: linearity, superposition, Thévenin's and Norton's theorems. Time-domain analysis: first and second order circuits, source-free and forced response. Sinusoidal steady-state analysis: phasors, complex power. Basic OpAmp circuitry.

**PRE OR COREQUISITES:** PHYS1202A/B or the former PHYS1302A/B; PHYS1402A/B; NMM1411A/B or the former AM1411A/B; NMM1412A/B or the former AM1412A/B; ES1036A/B or CS1026A/B (all prerequisites).

NMM2270A/B (corequisite).

Unless you have either the requisites for this course or written special permission from your Dean to enroll in it, you will be removed from this course and it will be deleted from your record.

**ANTIREQUISITES:** None.

**CEAB ACADEMIC UNITS:** Engineering Science 100%

LAB: None

TUTORIAL: Weekly, Remote and Asynchronous. Scheduled tutorial session

**RECOMMENDED/REQUIRED TEXT:** J. D. Irwin and R. M. Nelms, *Basic Engineering Circuit Analysis*, 11th ed., Hoboken, NJ: John Wiley & Sons, 2014. (Approximate cost: \$150)

**RECOMMENDED/ REQUIRED SOFTWARE:** There is no required software. Matlab (user license is available to all Western Students, software is also installed in general computer labs) or Numpy (free software) is recommended for solving matrix equations, and tutorials for using these will be provided in class materials. Students may, however, use any tool (software or otherwise) they wish to solve matrices.

# **RECOMMENDED RESOURCES/REFERENCES:** None.

# **GENERAL LEARNING OBJECTIVES (CEAB GRADUATE ATTRIBUTES)**

Knowledge Base	D	Engineering Tools	D	Impact on Society	
Problem Analysis	I	Individual & Teamwork		Ethics and Equity	
Investigation		Communication		Economics and Project Mgmt.	
Design		Professionalism		Life-Long Learning	

Notation: x represents the content level code as defined by the CEAB. blank = not applicable; I = introduced (introductory); D = developed (intermediate) and A = applied (advanced).

Rating: I – The instructor will introduce the topic at the level required. It is not necessary for the student to have seen the material before. D – There may be a reminder or review, but the student is expected to have seen and been tested on the material before taking the course. A – It is expected that the student can apply the knowledge without prompting (e. g. no review).

**COURSE MATERIALS:** Weekly lesson and tutorial content will be available on the course OWL site. Historical lesson content is available on OWL, but lessons are often updated and revised so attending the lectures is strongly recommended.

UNITS: SI

**COURSE TOPICS AND SPECIFIC LEARNING OUTCOMES:** The major learning outcome in this course is the ability to analyze and design linear electric circuits. This learning outcome is the cornerstone of many subsequent courses in electrical and mechatronics systems engineering.

The following table summarizes the course learning outcomes along with CEAB GAIs where the GAIs in bold indicate ones to be measured and reported annually.

Course Topics and Specific Learning Outcomes				
Electric Circuit Fundamentals				
At the end of this section, students will be able to:	KB3, PA1			
a. Define fundamental electrical properties including voltage, current, power, and resistance and state and apply mathematical relationships				
among those properties in simple circuits.				
b. Determine the equivalent resistance of series and parallel combinations of resistors.				
Apply Kirchoff's current law and Kirchoff's voltage law to analyze DC circuits consisting of voltage or current sources and resistors connected in a single loop or single node pair.				
Resistor Networks				
At the end of this section, students will be able to:	<b>KB3</b> , PA1,			
<ul> <li>a. Analyze DC linear circuits consisting of ideal and dependent voltage and/or current sources and resistor networks using both nodal and mesh analysis.</li> </ul>	ET1, <b>ET2</b>			
Analyze DC resistor networks using linear systems methods such as scaling,				
superposition, and Thévenin and Norton equivalent circuits.				
Operational Amplifier Circuits				
At the end of this section, students will be able to:  a. Analyze DC operational amplifier circuits using both the ideal op-amp model and an op-amp equivalent circuit model.  Analyze operational amplifier circuits exhibiting positive feedback, no	KB3, PA1			
feedback, and saturated outputs.				
Capacitors, Inductors, and RCL Circuits At the end of this section, students will be able to:	<b>KB3</b> , PA1,			
<ul> <li>Describe and explain the steady-state and transient behaviour of capacitors and inductors in circuits possessing DC sources.</li> <li>Derive and solve first- and second-order differential equations describing</li> </ul>	ET1, ET2			
time-domain transient responses of RC, RL, and RLC circuits.				
AC Analysis				
At the end of this section, students will be able to:	<b>KB3</b> , PA1,			
a. Understand the concept of root mean square values and phasors. Employ all of the techniques learned for DC analysis for AC circuits.	ET1, <b>ET2</b>			

# **EVALUATION:**

Name	% Worth	Assigned	Due Date	CEAB GAS ASSESSED
Homework	25%	Every two	Two weeks after	KB3, ET2
Assignments (5		weeks, starting	assignment	
total)		Monday,		

		September 15 <sup>th</sup>	date, posted on	
		15"	OWL	
Participation	5%	Monday of	Sunday of each	
Quizzes (10 total)		each week	week	
Midterm Tests (2	20%	To be	Two hours after	KB3
total)		determined	start	
Final Examination	50%	Scheduled by	Three hours	KB3, ET2
		OOR	after start	

Note that the dates listed above are **tentative** and may be adjusted if needed. Marks will be assigned on the basis of method of analysis and presentation, correctness of solution, clarity and neatness.

#### **COURSE POLICIES:**

All work submitted must be of professional quality in the requested format. Material that is handed in dirty, illegible, disorganized, or in an unapproved format will be returned to the student for resubmission and a late submission penalty may take effect.

**Tutorial Sessions:** The tutorials will present worked examples of solving the kinds of circuits that students may expect on homework assignments and the examinations. The tutorials are **optional** and will be online **only**. The scheduled tutorial session will, however, be used for the two in-person midterm tests.

**Homework Assignments:** Five homework assignments will be given. Each assignment will have some questions that are unique for each student (such as voltage values, circuit layout, transient behaviour, etc.). Students are welcome to work in groups, but it is each student's responsibility to ensure that the answers they submit correspond to the questions that they were asked. The homework assignments will be distributed on the course OWL site, and completed assignments will be submitted to OWL as well.

**Participation Quizzes:** Ten participation quizzes will be given, roughly one during each week of the term. These quizzes are short and may include multiple choice or true/false questions. They should pose no trouble to students who are keeping up with the course material. The purpose of these quizzes is to encourage students to maintain pace with the lectures. These quizzes will be completed online on the course OWL site.

**Midterm Examinations:** Two midterm tests will be scheduled during the regular academic term; the exact date will be determined later. Students will be notified of the test date through the course OWL site with no less than 2 weeks of advance notice. The tests will be held during the scheduled tutorial session in the classroom booked for the tutorial.

These midterm tests are **mandatory**, **closed-book**, **written** tests. If students miss a test and request academic consideration, there will be a make-up test the following week. If students are unable to attend that make-up test, another make-up will be scheduled. If a student is unable to write the test by the end of the semester, they will have the opportunity to write the test during the examination period. If a student is unable to write the test at all, they will receive zero for that assessment.

Please note that these midterm tests are considered to be central to the learning objectives for this course. Under no circumstances will the grade for either midterm test be reweighted to the final examination or the other midterm test. As noted above, make-up sessions will be provided for students who miss a test with good cause. Each test must be completed to avoid receiving a score of zero.

Students who miss multiple make-up sessions may expect the content of the test, when they eventually write it, to have evolved to stay reasonably concurrent with the course lectures.

**Final Examination**: The final exam will be scheduled by the Office of the Registrar during the final examination period. Details on the location, mode of delivery, and allowed aids will be posted in advance.

To obtain a passing grade in the course, a mark of 50% or more must be achieved on the final examination. A final examination mark < 50% will result in a final course grade of 48% or less. If the above conditions are not met, your final grade cannot be greater than 48%. Students who have failed this course (i.e., final average < 50%) must repeat all components of the course.

**Assignment Submission Locker:** Submission of any and all course work will be done online using OWL. A submission locker will not be used.

## **USE OF GENERATIVE AI POLICY:**

Students will have the opportunity to use computational tools for analyzing and designing circuits on the homework assignments and the final examination. It is perfectly permissible to use generative AI (genAI) as a tool to help complete these assessments, but it is very poor engineering practice to rely entirely on genAI. Consequently, any student who submits work that was 100% produced by genAI will receive **zero part marks** for that question. If the question was answered correctly by genAI, the student will receive the full grade – but if the genAI made mistakes (as it often does), then the student will receive a zero for that question. The course instructor **will not** use other genAI tools to assess for genAI use by students – rather the course instructor will assess whether a student relied entirely on genAI by checking if that student's submitted answers contains obvious AI prompts and text. Students who make heavy use of genAI must, at a minimum, read the genAI output and make necessary edits to ensure it fully addresses the question that was asked.

## LATE SUBMISSION POLICY:

This course employs flexible deadlines for homework assignments and participation quizzes. The homework assignment and participation quiz deadlines will be posted on OWL well in advance of the due date. For each assessment, students are expected to submit their final answers by the deadline listed. Should illness or extenuating circumstances arise, students are permitted to submit their final answers up to 48 hours past the deadline without academic penalty. Late submissions will not be accepted without permission from the course instructor. Should students miss the flexible deadline, they should contact the course instructor by email to resolve the situation. As flexible deadlines are used in this course, requests for academic consideration will not be granted.

If you have a long-term academic consideration or accommodation for disability that allows greater flexibility than provided here, please reach out to your instructor at least one week prior to the posted deadline.

ATTENDANCE: Attendance is mandatory for all lectures.

## **FACULTY OF ENGINEERING POLICIES:**

Students must familiarize themselves with the policies of the Faculty of Engineering https://www.eng.uwo.ca/electrical//pdf/2025-UG-Policy-and-Procedures.pdf