

Western University
Faculty of Engineering
Department of Electrical and Computer Engineering
ECE 3349 - Introduction of VLSI
Course Outline Fall/Winter 2026

COURSE DESCRIPTION: This course is an introduction to concepts associated with the analysis and design of integrated circuits (IC) in the state-of-the-art CMOS technologies. Continuous advances in microelectronics and Very Large Scale of Integration (VLSI) made an entire electronic system on a single chip (SoC) possible. Modern VLSI ICs contain more than two billion components per chip. Design and manufacturing of semiconductor devices present unique challenges, especially at the conceptual and design levels, therefore computer-assisted design (CAD) methods are sought to help manage these complex designs. In particular, this course introduces CMOS semiconductor devices, physical principles behind IC design, design and analysis of digital logical gates, and the use of professional CAD tools for IC design.

ACADEMIC CALENDAR:

https://www.westerncalendar.uwo.ca/Courses.cfm?CourseAcadCalendarID=MAIN_017636_1&SelectedCalendar=Live&ArchiveID=

This course covers fundamentals of semiconductor physics as applied to microelectronics, theory of semiconductor materials and devices. Students will be exposed to basic elements of CMOS circuitry design, including practical implementation of resistors, capacitors, diodes, transistors and MOSFET. Related topics such as delays, cross-talk, parasitics, temperature effects are included.

PRE OR COREQUISITES: ES1021A/B, ECE2233A/B, ECE2236A/B, ECE2240A/B, ECE2241A/B, ECE2277A/B, ECE2238A/B and successful completion of the second year of the Electrical or Computer Engineering program or Integrated Engineering Program.

Unless you have either the requisites for this course or written special permission from your Dean to enroll in it, you will be removed from this course and it will be deleted from your record. This decision may not be appealed. You will receive no adjustment to your fees in the event that you are dropped from a course for failing to have the necessary prerequisites.

ANTREQUISITES: None.

CEAB ACADEMIC UNITS: Engineering Science 100%

INSTRUCTOR INFORMATION:

Instructor:

Office:

Phone:

Email:

CONTACT HOURS: Timetable information is available at <http://draftmyschedule.uwo.ca/>.

Lectures occur weekly starting September 9th.

LECTURE:

LAB:

TUTORIAL:

RECOMMENDED/REQUIRED TEXT: There is no required textbook. The recommended textbook is H. E. Neil and D. Harris, *CMOS VLSI Design, A Circuits and Systems Perspective*, Pearson Education, 4th Edition (2011). E-book copies can be rented from the publisher for \$79.99.

RECOMMENDED/REQUIRED SOFTWARE: Cadence OrCAD or SPICE will be required to complete the labs. The exact software required is still being determined. Students will have access to the software through their student credentials.

RECOMMENDED RESOURCES/REFERENCES: Any further recommended reading will be posted on OWL.

GENERAL LEARNING OBJECTIVES (CEAB GRADUATE ATTRIBUTES)

Knowledge Base	D	Use of Engineering Tools		Impact on Society and the Environment	
Problem Analysis		Individual and Team Work		Ethics and Equity	
Investigation	A	Communication Skills	A	Economics and Project Management	
Design		Professionalism		Life-Long Learning	

Notation: where x be I: Introductory, D: Intermediate, A: Advanced, or empty. I – The instructor will introduce the topic at the level required. It is not necessary for the student to have seen the material before. D – There may be a reminder or review, but the student is expected to have seen and been tested on the material before taking the course. A – It is expected that the student can apply the knowledge without prompting (e.g. no review).

COURSE MATERIALS: Weekly lesson content will be available on the course OWL site.

UNITS: SI

COURSE TOPICS AND SPECIFIC LEARNING OUTCOMES: The major learning outcome in this course is the ability to analyze and design linear electric circuits. This learning outcome is the cornerstone of many subsequent courses in electrical and mechatronics systems engineering.

The following table summarizes the course learning outcomes along with CEAB GAIs where the GAIs in bold indicate ones to be measured and reported annually.

Course Topics and Specific Learning Outcomes	CEAB Graduate Attributes Indicators
Semiconductor Devices and Technology Section covers electrical properties of doped silicon; NMOS, PMOS, and CMOS architectures; and an overview of IC fabrication. At the end of this section, students will be able to: a. Understand the physical and engineering principles behind semiconductor technology. b. Understand CMOS processing steps.	KB3, CS1
CMOS Logic Section covers basic CMOS logic circuits; compound gates; signal strength and propagation; CMOS latches and flip-flops; timing and clock skew; gate layout; and stick diagrams. At the end of this section, students will be able to: a. Understand theoretical principles behind CMOS logic gates. b. Understand CMOS circuits and layouts. c. Design and test functionality of basic gates by using CAD tools.	KB3, I2
MOS Transistor Theory Section covers current-voltage operation of MOS transistors; real-world effects and capacitance; channel formation; operation in cutoff, linear, and saturation regions; DC response and load-line analysis; DC transfer curves; noise margins; and logic levels. At the end of this section, students will be able to: a. Understand theoretical principles behind MOS device operation. b. Understand practical engineering issues related to MOS device	KB3

design. c. Solve basic MOS circuits using simple models for MOS operation.	
Transient Response Section covers transient response of MOS transistors; propagation delays; rise and fall times; simple models of MOS delay; and small signal analysis using equivalent circuits. At the end of this section, students will be able to: a. Understand DC and transient response of transistors. b. Solve transient response of basic MOS circuits using simple models and equivalent circuits.	KB3
Logical Effort Section covers delay models to inform chip design; logical and electrical effort; delay paths in multistage networks; designing fast circuits; selecting optimal number of stages in a multistage circuit; and stage effort sensitivity analysis. At the end of this section, students will be able to: a. Understand delay, logical effort, and principles of designing fast ICs. b. Solve for the delay in multistage networks. c. Design optimized multistage circuits.	KB3, I2
Power Section covers instantaneous and average power; heat dissipation; switching waveforms; dynamic power reduction; activity factors and techniques for estimating them; sources of power leakage; and static power. At the end of this section, students will be able to: a. Understand different sources of power dissipation. b. Solve for power consumption of ICs. c. Design low-power ICs.	KB3
Combinational and Sequential Circuit Design Section covers bubble pushing; compound gates; different circuit families; sequencing for static and dynamic circuits; and circuit design of latches and flip-flops. At the end of this section, students will be able to:	KB3

a. Understand techniques to optimize combinational circuits for lower delay and/or power. b. Understand sequencing for both static and dynamic circuits. c. Understand circuit families and design of latches and flip-flops.	
Circuit Simulation Section covers modeling and simulating circuits using Cadence and SPICE; verifying IC operation; and designing ICs for specific performance requirements. This course topic will be primarily addressed in the laboratory exercises. At the end of this section, students will be able to: a. Synthesize and analyze a basic digital logic IC. b. Design and verify IC operation using Analog Cadence tools and a SPICE simulator.	I2

EVALUATION:

Note that the dates listed above are **tentative** and may be adjusted if needed. Marks will be assigned on the basis of method of analysis and presentation, correctness of solution, clarity and neatness.

Course Component	Weight	Assigned	Due Date	CEAB GAS ASSESSED
Homework Assignments (4 total)	20%			KB3
Laboratory (4 total)	20%			KB3, I2, CS1
Midterm Test	10%			
Final Examination	50%			KB3

COURSE POLICIES:

To obtain a passing grade in the course, a mark of 50% or more must be achieved on the final examination as well as on the laboratory. A final examination or laboratory mark < 50% will result in a final course grade of 48% or less.

All work submitted must be of professional quality in the requested format. Material that is

handed in dirty, illegible, disorganized, or in an unapproved format will be returned to the student for resubmission and a late submission penalty may take effect.

Homework Assignments: Assignments will be regularly announced and posted on the course OWL site. Students must provide their answers on OWL as instructed on the assignment and by the posted due date. These assignments will be problem based.

Laboratory: This course has four lab exercises. Lab exercises are based on simulation and can be completed asynchronously and remotely. Labs must be completed individually. Laboratory reports should be submitted online using OWL by the posted due date.

Midterm Test: The midterm test will be scheduled during the regular academic term; the exact date will be determined later. Students will be notified of the test date and location through the course OWL site with no less than 2 weeks of advance notice. The midterm test will be an in-person, closed-book test. The midterm test is **optional**, if students do not complete the midterm, that portion of their grade will be added to the final examination.

Final Examination: The final examination will take place during the regular examination period, as scheduled by the registrar. The final exam will be an in-person, closed-book test. The final examination will cover all content discussed in the lessons. If a student receives a higher grade on their final exam than on their midterm exam, the midterm grade will be discarded, and the final exam grade will be used in its stead.

Late Submission Policy: Homework Assignments should be submitted by the posted deadlines. Accommodations for late submission might be made at student's request (assuming this request is made in a timely manner) at the instructor's discretion. The priority will be marking submitted assignments and posting the answers to OWL reasonably promptly after the assignment deadline as a study aid for students. No late assignments will be accepted, for any reason, after the answers are posted. Students should complete laboratory exercises according to the posted schedule. Students must contact the instructor promptly if they are unable to meet a laboratory submission deadline and seek an accommodation. Laboratory assignments will generally not be accepted after the posted deadline unless an accommodation is granted for exceptional circumstances.

Assignment Submission Locker: Submission of any and all course work (homework, lab reports) will be done online using OWL. A submission locker will not be used.

USE OF GENERATIVE AI POLICY:

Students will have the opportunity to use computational tools for analyzing and designing circuits on the homework assignments and any take-home tests. It is perfectly permissible to use generative AI (genAI) as a tool to help complete these assessments, but it is very poor engineering practice to rely entirely on genAI. Consequently, any student who submits work

that was 100% produced by genAI will receive **zero part marks** for that question. If the question was answered correctly by genAI, the student will receive the full grade – but if the genAI made mistakes (as it often does), then the student will receive a zero for that question. The course instructor **will not** use other genAI tools to assess for genAI use by students – rather the course instructor will assess whether a student relied entirely on genAI by checking if that student's submitted answers contains obvious AI prompts and text. Students who make heavy use of genAI must, at a minimum, read the genAI output and make necessary edits to ensure it fully addresses the question that was asked.

LATE SUBMISSION POLICY:

This course employs flexible deadlines for homework assignments and participation quizzes. The homework assignment and participation quiz deadlines will be posted on OWL well in advance of the due date. For each assessment, students are expected to submit their final answers by the deadline listed. Should illness or extenuating circumstances arise, students are permitted to submit their final answers up to 48 hours past the deadline without academic penalty. Late submissions will not be accepted without permission from the course instructor. Should students miss the flexible deadline, they should contact the course instructor by email to resolve the situation. **As flexible deadlines are used in this course, requests for academic consideration will not be granted.**

If you have a long-term academic consideration or accommodation for disability that allows greater flexibility than provided here, please reach out to your instructor at least one week prior to the posted deadline.

ATTENDANCE: Attendance is mandatory for all lectures.

FACULTY OF ENGINEERING POLICIES:

Students must familiarize themselves with the policies of the Faculty of Engineering.

[Policies and Procedures for Undergraduate Students.](#)